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Wide-range single-ended CMOS track-and-hold circuit

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Abstract: This paper investigates the performance of a MOS track-and-hold circuit as the front end of a wide input range and high-speed single-sided ADC. In order to reduce charge injection and clock feedthrough errors, a new technique for employing a dummy transistor in the bootstrapped switch of the track and hold circuit is introduced. Performance of the proposed circuit for the two cases of constant and non-linear hold capacitor is studied. It is also shown that how and when dummy switch and bulk switching method can improve the accuracy of the T/H.

Keywords: track and hold, static error, total harmonic distortion

Classification: Integrated circuits

References

[1] M. Dessouky and A. Kaiser, "Very Low-Voltage Digital-Audio ΣΔModulator with 88-dB Dynamic Range Using Local Switch Bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, pp. 349–355, March 2001.

[2] T. S. Lee and C. C. Lu, "A 1.5 V 50-MHz pseudo-differential sample-and-hold circuit with low hold pedestal," *IEEE Trans. Circuits and Syst.I*, vol. 52, pp. 1752–1757, Sept. 2005.

[3] C. J. B. Fayomi, G. W. Roberts, and M. Sawan, "Low-Voltage CMOS Analog Bootstrapped Switch for Sample-and-Hold Circuit," *Proc. IEEE Int. Symp. Circuits Syst.*, pp. 2200–2203, May 2005.

[4] F. Centurelli, P. Monsurro, and A. Trifiletti, "A model for the distortion due to switch on-resistance in sample-and-hold circuits," *Proc. IEEE Int. Symp. Circuits Syst.*, pp. 4787–4790, May 2006.

[5] M. Waltari and K. Halonen, "Bootstrapped switch without body effect in standard CMOS technology," *IEEE Electron. Lett.*, vol. 38, pp. 555–557, 2002.

[6] H. Movahedian, M. Azin, and M. Sharif Bakhtiar, "A Low Voltage Low Power 8-bit Folding/Interpolating ADC with rail-to-rail Input Range," *Proc. IEEE Int. Symp. Circuits Syst.*, pp. I-77–80, May 2004.

1 Introduction

Track-and-Hold (T/H) circuits play an important role in the design of analog to digital converters (ADC) especially at high sampling rates. Although the

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closed-loop track and holds provide higher precision, open-loop T/H's are usually preferred in high speed applications. An open-loop T/H is basically comprised of a MOS switch and a hold capacitor. In low voltage circuits, clock bootstrapping is often utilized to increase the overdrive voltage of the MOS switch. Moreover, bootstrapping has the advantages of reducing the variation of the on-resistance of the switch transistor and also making charge injection of the switch signal-independent [1]. For a wide input range T/H, however, additional techniques such as bulk effect cancellation and the use of dummy switch may be required to improve the accuracy.

The body effect of the sampling switch results in signal-dependent on-resistance (R_{ON}) of the switch during the tracking phase. The resulting non-linear time constant ($R_{ON}.C_H$), is the main source of distortion at high input frequencies [2]. If the process provides the possibility to have NMOS transistors with isolated bulk, the problem can be mitigated by connecting the bulk of the main switch to the input node during the tracking phase, canceling the body effect [1]. In the hold phase, the bulk is connected to the ground in order to prevent negative source-to-bulk voltage. Fig. 1 (a) shows the circuit for body effect cancellation.

When a T/H is placed directly in the front end of an ADC, all or a part of the hold capacitor is the input capacitance of the ADC. The input capacitance of a flash or folding ADC is, in general, signal-dependent. The same way as for the resistance of the switch, a signal-dependent hold capacitor makes the tracking time-constant nonlinear and generates distortion. Moreover, as the clock feed-through error is a function of the hold capacitor, the nonlinearity of the hold capacitor causes the clock feed-through error to be nonlinear, hence, increasing the distortion, especially the second harmonic. Although the second harmonic can be reduced in differential circuits, in single-ended applications it is the major source of non-linearity.

This paper presents a new method for realization of dummy MOS switch for bootstrapped switches. Furthermore, impact of both bulk effect cancellation and dummy switch on the performance of the T/H is investigated. It will be shown that the proposed dummy switch considerably reduces the static error of the T/H and it is indeed an effective approach in reducing the distortion of T/H in presence of a non-constant hold capacitor.

2 Realization of dummy switch

Using a dummy switch with proper size is a common practice to reduce the pedestal error caused by charge injection and clock feedthrough in switched-capacitor circuits. For a bootstrapped NMOS switch, the gate voltage drops from $V_{DD} + V_{in}$ to ground at the end of the tracking phase. To cancel out the effect of this transition on the sampled signal, two methods have been previously reported [2, 3] as shown in Fig. 1. In the circuit of Fig. 1 (b) [2], gate voltage of the dummy switch (M_D) changes from zero to V_{out} ($=V_{in}$) at the beginning of the hold phase. This would cancel the signal-dependent part of the error caused by clock feed-through. However, charge sharing between

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the hold capacitor and parasitic capacitances of M_1 and M_2 will degrade the accuracy of the circuit. Furthermore this method is only applicable when the maximum input/output voltage is sufficiently lower than V_{DD} otherwise M_2 will not turn on. The circuit in Fig. 1 (c) [3] does not suffer from these difficulties, but the gate voltage of the dummy switch (M_D) tracks the input voltage in the hold phase and a capacitive coupling between input and output is created. This degrades the accuracy of the circuit especially when sampling a high frequency input signal.

For optimum operation of the dummy switch, the bootstrapping circuit of the dummy transistor must sense a voltage equal to the sampled output voltage. Connecting the bootstrapping circuit to the output node causes charge transfer between the hold capacitor and the capacitor of the bootstrapping circuit which would be a new source of pedestal error. Using a buffer solves the problem but such a buffer would require a wide input range and very high bandwidth, increasing both complexity and power consumption. A low-power solution, proposed in Fig. 1 (d), is to use an auxiliary T/H to generate a replica of the main output voltage and apply this voltage to the bootstrapping circuit of the dummy switch. In this way, the dummy bootstrapping circuit is completely isolated from the output node. The gate voltage of the dummy switch changes from zero to $V_{DD}+V_{in}$ canceling the clock feed-through and charge injection effects of the main switch to a high degree.

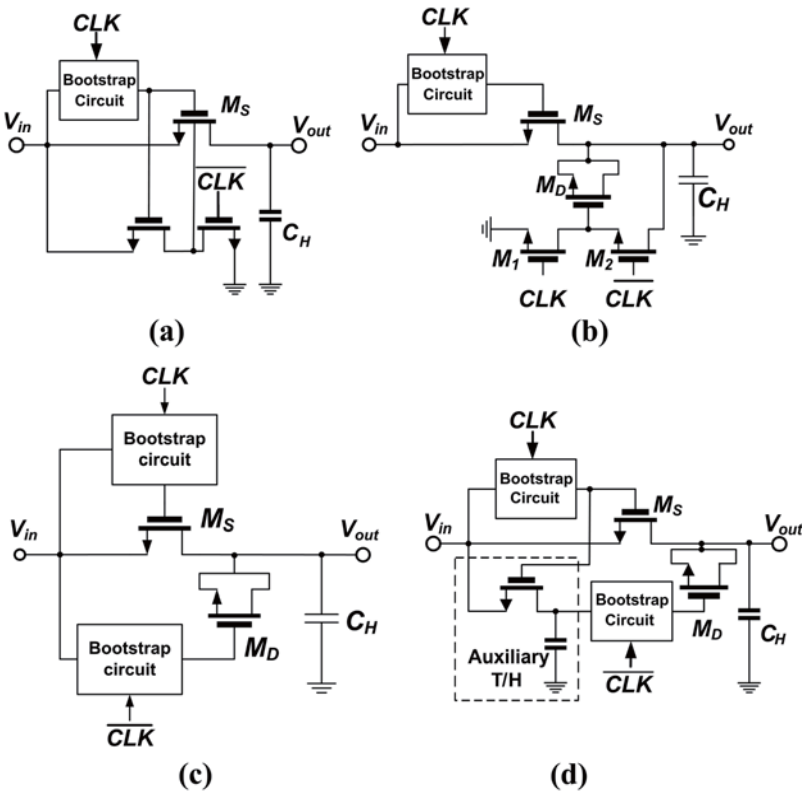

Fig. 1. (a) Bootstrapped switch without bulk effect, (b) Sampled output used for bootstrapped dummy, (c) Bootstrapped dummy, (d) Proposed auxiliary T/H used for bootstrapped dummy

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3 Results and Discussion

For a single-ended T/H circuit with a supply voltage of 1.5 V and 1.1 Vpp input range, two sets of simulations were performed; one with DC input to evaluate the static (pedestal) error and one with a variety of full-scale sine inputs to estimate the dynamic performance. Each simulation was repeated for the following cases:

Case1: Bootstrapped switch without dummy transistor and without bulk switching,

Case2: Bootstrapped switch without dummy transistor and with bulk switching,

Case3: Bootstrapped switch with dummy transistor as in Fig. 1 (d) and without bulk switching,

Case4: Bootstrapped switch with both dummy transistor and bulk switching.

Simulations were performed using BSIM3v3 model for transistors and the bootstrapping circuit is similar to that of [1].

Static error: The simulation results for the static error versus input voltage are shown in Fig. 2. As it can be seen, using a dummy transistor improves the static error by one order of magnitude whereas bulk switching has no improving effect on the pedestal error. In effect, it causes an input-dependent error. The reason is that at the falling edge of the bootstrapped clock of the main switch, the bulk voltage of this switch jumps from V_{in} to V_{ss}. This will cause a sudden change of the threshold voltage and consequently the change of the channel charge.

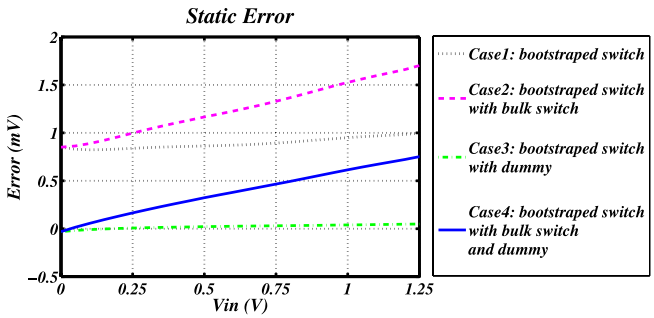

Fig. 2. Static error vs. input voltage

Dynamic performance: The effect of each technique on improving THD is studied once with a constant hold capacitance and then with the nonlinear capacitance of the ADC for which the T/H is designed. The impact of dummy/bulk switches on the second and third harmonics is shown in Fig. 3 (a) for a constant hold capacitor. As it can be seen, the dummy has no improving effect on dynamic performance whereas bulk switch effectively changes the shape of the harmonic distortions. On the one hand, bulk switching reduces the frequency-dependent part of the second and third harmonics. On the other hand, the sudden change of threshold voltage makes a nonlinear charge injection error which results in an additional constant offset in the second and third harmonics. As a result, in lower frequencies the use of

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the bulk switching degrades the THD while at higher frequencies it has an improving effect.

Replacing the constant capacitor by a nonlinear input capacitance of an ADC [6], the 2nd and 3rd harmonics are recalculated as shown in Fig. 3 (b). Distortion due to nonlinear hold capacitance has two components; one due to signal-dependent clock feed-through and charge injection which is independent of the input frequency and one due to the nonlinear time constant whose amplitude is proportional to the frequency of the input signal. The shape of the second harmonic distortion (HD2) for the case 1 suggests that at lower frequencies, HD2 is determined by the clock feed-through and charge injection while at higher frequencies the nonlinear time constant is the dominant factor. For the case 2, the overall shape of HD2 is the same as case 1, but due to the constant switch resistance, the corner frequency (i.e. the frequency where the two components of HD2 are equal) shifts toward higher frequencies. Using dummy switch effectively removes the first component and improves HD2 at low frequencies. Using both techniques simultaneously (case4), improves the HD2 from more than 20 dB at low frequencies up to 8 dB at nyquist frequency (50 MHz in this case). Comparing the third harmonic distortion of the four cases with the third harmonic of an RC network with a nonlinear C ($= C_H$) reveals that even at low frequencies the nonlinear C_H is the dominant cause of HD3. As expected, neither of the techniques can cancel this effect and HD3 remains almost unchanged.

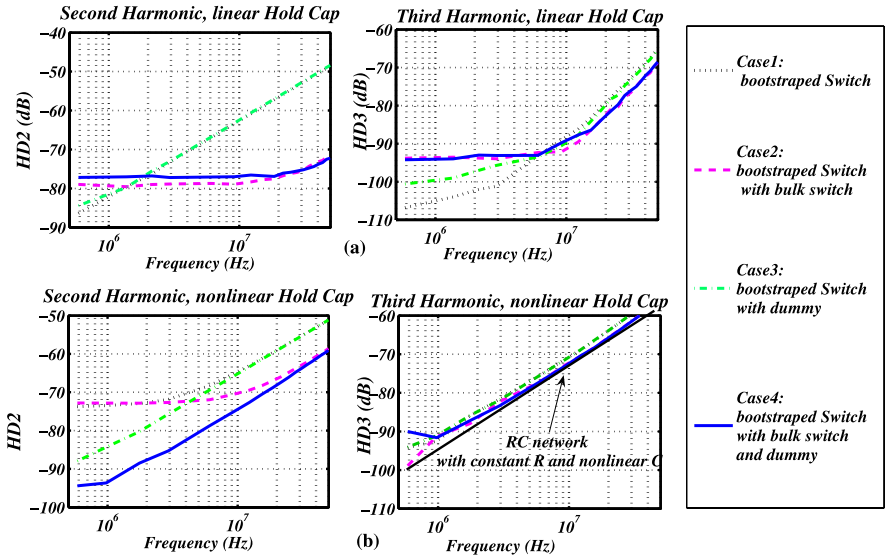

Fig. 3. Second and third harmonics vs. input Frequency
(a) Linear CH, (b) Nonlinear CH

As mentioned earlier, while HD2 can be reduced by differential operation, some applications such as [6] impose the use of single-ended T/H. Moreover, even with differential circuits, cancellation of HD2 is not perfect because of the mismatch between two half-circuits. Consequently, using the proposed method in differential circuits relax the matching requirements between the

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half-circuits.

4 Conclusion

Introducing a new technique for incorporating dummy switch in bootstrapped T/H circuits, the effects of using dummy switch as well as bulk switching on static and dynamic errors of open-loop T/H were investigated in this paper. It was shown that for the best static and dynamic performance, both bulk switching and dummy switch need to be used, especially for the case of a nonlinear hold capacitor.

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